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Performance analysis of an efficient Physically Unclonable Function architecture using CNTFET technology

ABSTRACT. In this era of technological development, Internet of Things (IoT) applications play an important role. IoT has been leaving its impression on almost every set of applications like commercial, consumer, infrastructure spaces and industrial purposes. With increasing applications of IoT in day-to-day life, data vulnerability has also been increasing Physically unclonable functions (PUFs) have emerged as an efficient security solution to the stumbling block of physical attack on IoT devices. PUFs have the potential to generate specific identifiers without the concern of storing the key and sensitive information like in cryptography. Nevertheless the power, uniqueness and robustness of PUF create challenges in its implementation. The ring oscillator PUF (RO PUF) has limited applications because of its power budget. Hence, a low power-adapted RO PUF could be very useful. This paper proposes an ultralow power RO PUF. The architecture presented has age resilience, which provides more reliability. A total simulation has been carried out with HSPICE software. Primarily, the architecture has been implemented over 130 nm MOSFET technology, then over 32 nm MOSFET technology, and finally over 32 nm CNTFET technology. The corresponding values of power, delay and power delay product have been measured and tabulated. The observations show the variance of the measured values over their simulation on the three technologies. The proposed architecture achieves an efficiency of 88.45%.

Keywords: CNTFET, HSPICE, PUF, RO PUF, ultralow power

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